

WHAT IS CLAIMED IS:

1.     An apparatus for providing an input output from an  
5     integrated circuit, the apparatus comprising:

        an input/output (I/O) pad;

        an upper pair of P-channel Metal Oxide Semiconductor  
        (PMOS) devices, a first of the upper PMOS devices having  
        source coupled to a power supply ( $V_{DD0}$ ) and drain coupled to  
10     source of a second upper PMOS device, the second PMOS device  
        having drain coupled to the I/O pad;

        a lower pair of N-channel MOS devices (NMOS), a first of  
        the upper NMOS devices having a drain coupled to the I/O pad  
        and a source coupled to a drain of a second lower NMOS device,  
15     the second NMOS device having a source coupled to a ground  
        potential;

        a first bias circuit coupled to a gate of the first upper  
        PMOS device, said bias circuit providing a first bias voltage  
        to the gate of the first upper PMOS device when the I/O pad is  
20     in an output mode and  $V_{DD0}$  voltage otherwise;

        a second bias circuit coupled to a gate of the second  
        lower NMOS device, said bias circuit providing a second bias  
        voltage to the gate of the second lower NMOS device when the  
        I/O pad is in an output mode and a ground voltage otherwise;

25     a third bias circuit coupled to a gate of the second  
        upper PMOS device, said bias circuit providing a third bias  
        voltage, coupled to the gate of the second upper MOS device;  
        and

        a fourth bias circuit coupled to a gate of the first  
30     lower NMOS device, said bias circuit providing a fourth bias  
        voltage to the gate of the first lower MOS device, the fourth  
        bias voltage being in a range, the range having a maximum  
        value of  $V_{DDP} + V_T$  and a minimum value of  $(V_{DD0} - V_{Tp})$ , where  $V_{DDP}$   
        and  $V_{DD0}$  are power supply voltages and  $V_T$  and  $V_{Tp}$  are offset  
35     voltages.

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2.     The apparatus of claim 1 wherein  $V_{DD0}$  and  $V_{DDP}$  are the same power supply.

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3.     The apparatus of claim 1 wherein  $V_T$  and  $V_{Tp}$  are the same offset voltages.

4.     An apparatus for providing an input output from an integrated circuit, the apparatus comprising:

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an input/output (I/O) pad;

an upper pair of P-channel Metal Oxide Semiconductor (PMOS) devices, a first of the upper PMOS devices having source coupled to a power supply ( $V_{DD0}$ ) and drain coupled to source of a second upper PMOS device, the second PMOS device having drain coupled to the I/O pad;

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a lower pair of N-channel MOS devices (NMOS), a first of the upper NMOS devices having a drain coupled to the I/O pad and a source coupled to a drain of a second lower NMOS device, the second NMOS device having a source coupled to a ground potential;

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a first bias circuit coupled to a gate of the first upper PMOS device, said bias circuit providing a first bias voltage to the gate of the first upper PMOS device when the I/O pad is in an output mode and  $V_{DD0}$  voltage otherwise;

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a second bias circuit coupled to a gate of the second lower NMOS device, said bias circuit providing a second bias voltage to the gate of the second lower NMOS device when the I/O pad is in an output mode and a ground voltage otherwise;

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a third bias circuit coupled to a gate of the second upper PMOS device, said bias circuit providing a third bias voltage to the gate of the second upper MOS device; and

a fourth bias circuit coupled to a gate of the first lower NMOS device, said bias circuit providing a fourth bias voltage to the gate of the first lower MOS device depending on

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the voltage on the I/O pad ( $V_{PAD}$ ) when the pad is in an output  
disable mode, and said bias circuit providing a fixed fourth  
5      bias voltage to the gate of the first lower MOS device when  
the pad is in an output enable mode.

10      5. The apparatus of claim 4 wherein the fixed fourth  
bias voltage is  $V_{DDP}$ .

10      6. An apparatus for providing an input output from an  
integrated circuit, the apparatus comprising:

an input/output (I/O) pad;

15      an upper pair of P-channel Metal Oxide Semiconductor  
(PMOS) devices, a first of the upper PMOS devices having  
source coupled to a power supply ( $V_{DDO}$ ) and drain coupled to  
source of a second upper PMOS device, the second PMOS device  
having drain coupled to the I/O pad;

20      a lower pair of N-channel MOS devices (NMOS), a first of  
the upper NMOS devices having a drain coupled to the I/O pad  
and a source coupled to a drain of a second lower NMOS device,  
the second NMOS device having a source coupled to a ground  
potential;

25      a first bias circuit coupled to a gate of the first upper  
PMOS device, said bias circuit providing a first bias voltage  
to the gate of the first upper PMOS device when the I/O pad is  
in an output mode and  $V_{DDO}$  voltage otherwise;

30      a second bias circuit coupled to a gate of the second  
lower NMOS device, said bias circuit providing a second bias  
voltage to the gate of the second lower NMOS device when the  
I/O pad is in an output mode and a ground voltage otherwise;

35      a third bias circuit coupled to a gate of the second  
upper PMOS device, said bias circuit providing a third bias  
voltage to the gate of the second upper MOS device equal to  
the voltage on the I/O pad ( $V_{PAD}$ ) when the pad is in an output

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disable mode, and where the third bias voltage to the gate of the second upper MOS device equal to a fixed voltage when the pad is in an output enabled mode; and

5           a fourth bias circuit coupled to a gate of the first lower NMOS device, said bias circuit providing a fourth bias voltage to the gate of the first lower MOS device.

10           7.    The apparatus of claim 6 wherein the fixed voltage is  $V_{DDC}$ .

8.    An apparatus for providing an input output from an integrated circuit, the apparatus comprising:

15           an input/output (I/O) pad;

          an upper pair of P-channel Metal Oxide Semiconductor (PMOS) devices, a first of the upper PMOS devices having source coupled to a power supply ( $V_{DD0}$ ) and drain coupled to source of a second upper PMOS device, the second PMOS device having drain coupled to the I/O pad;

20           a lower pair of N-channel MOS devices (NMOS), a first of the upper NMOS devices having a drain coupled to the I/O pad and a source coupled to a drain of a second lower NMOS device, the second NMOS device having a source coupled to a ground potential;

25           a first bias circuit coupled to a gate of the first upper PMOS device, said bias circuit providing a first bias voltage to the gate of the first upper PMOS device when the I/O pad is in an output mode and  $V_{DD0}$  voltage otherwise;

30           a second bias circuit coupled to a gate of the second lower NMOS device, said bias circuit providing a second bias voltage to the gate of the second lower NMOS device when the I/O pad is in an output mode and a ground voltage otherwise;

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          a third bias circuit coupled to a gate of the second  
upper PMOS device, said bias circuit providing a third bias  
5       voltage to the gate of the second upper MOS device; and

          a fourth bias circuit coupled to a gate of the first  
lower NMOS device, said bias circuit providing a fourth bias  
voltage to the gate of the first lower MOS device depending on  
the voltage on the I/O pad ( $V_{PAD}$ ), said fourth bias circuit  
10       comprising a capacitive voltage divider.

          9. The apparatus of claim 8 wherein the capacitive  
voltage divider proportions the difference between a pad and  
power supply voltage to derive the fourth bias voltage, when a  
15       voltage provided to the pad is changing.

          10. An apparatus for providing an input output from an  
integrated circuit, the apparatus comprising:

          an input/output (I/O) pad;  
20       an upper pair of P-channel Metal Oxide Semiconductor  
(PMOS) devices, a first of the upper PMOS devices having  
source coupled to a power supply ( $V_{DD0}$ ) and drain coupled to  
source of a second upper PMOS device, the second PMOS device  
having drain coupled to the I/O pad;

25       a lower pair of N-channel MOS devices (NMOS), a first of  
the upper NMOS devices having a drain coupled to the I/O pad  
and a source coupled to a drain of a second lower NMOS device,  
the second NMOS device having a source coupled to a ground  
potential;

30       a first bias circuit coupled to a gate of the first upper  
PMOS device, said bias circuit providing a first bias voltage  
to the gate of the first upper PMOS device when the I/O pad is  
in an output mode and  $V_{DD0}$  voltage otherwise;

          a second bias circuit coupled to a gate of the second  
35       lower NMOS device, said bias circuit providing a second bias

voltage to the gate of the second lower NMOS device when the I/O pad is in an output mode and a ground voltage otherwise;

5            a third bias circuit coupled to a gate of the second upper PMOS device, said bias circuit providing a third bias voltage to the gate of the second upper MOS device depending on the voltage on the I/O pad ( $V_{PAD}$ ) said third bias circuit comprising a capacitive voltage divider; and

10           a fourth bias circuit coupled to a gate of the first lower NMOS device, said bias circuit providing a fourth bias voltage to the gate of the first lower MOS device.

15           11. The apparatus of claim 10 wherein the capacitive voltage divider proportions a difference in voltage at the pad and a power supply voltage to derive the third bias voltage when the pad is switching.

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